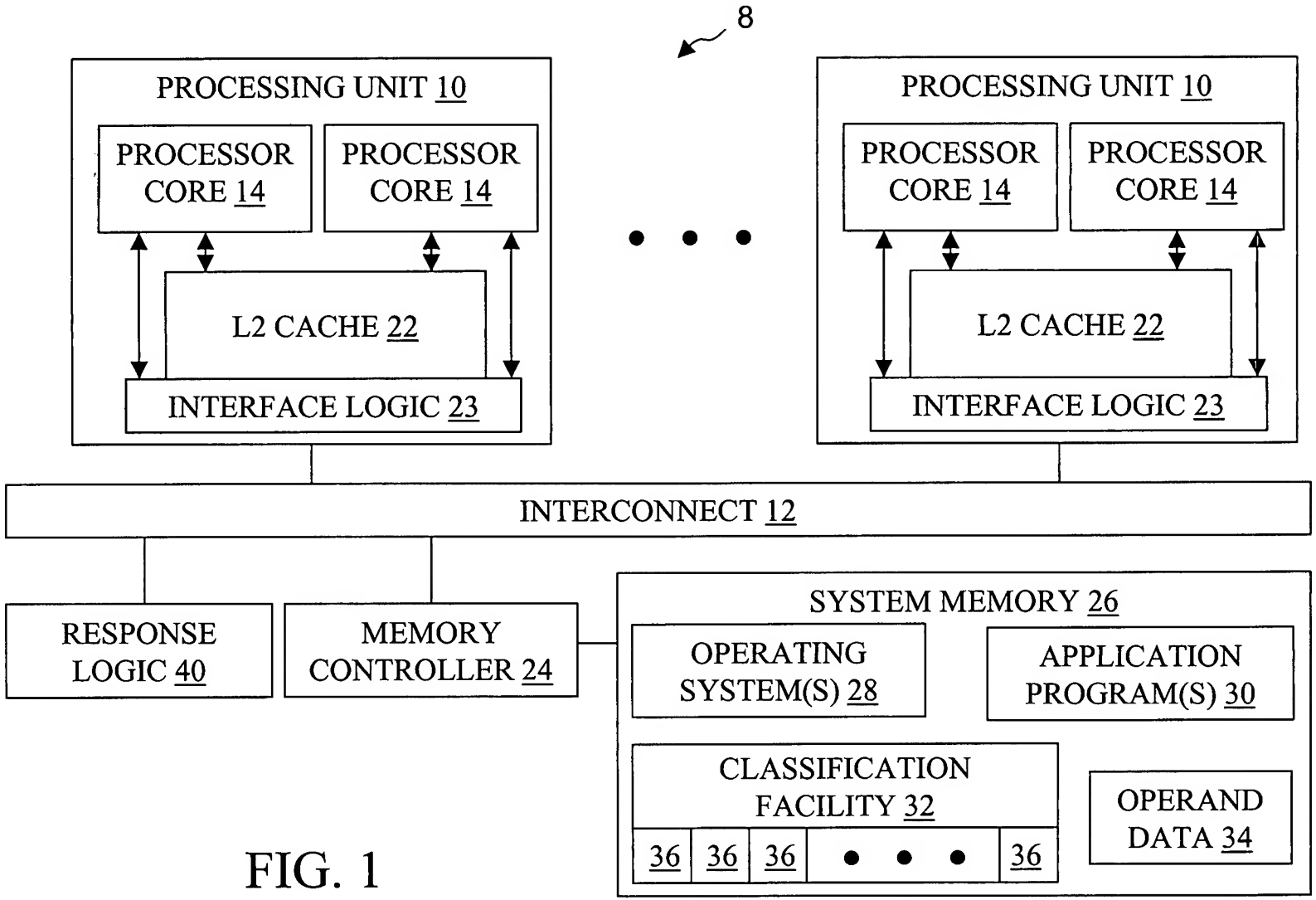


FIG. 1

US9200720071S1 D716906S

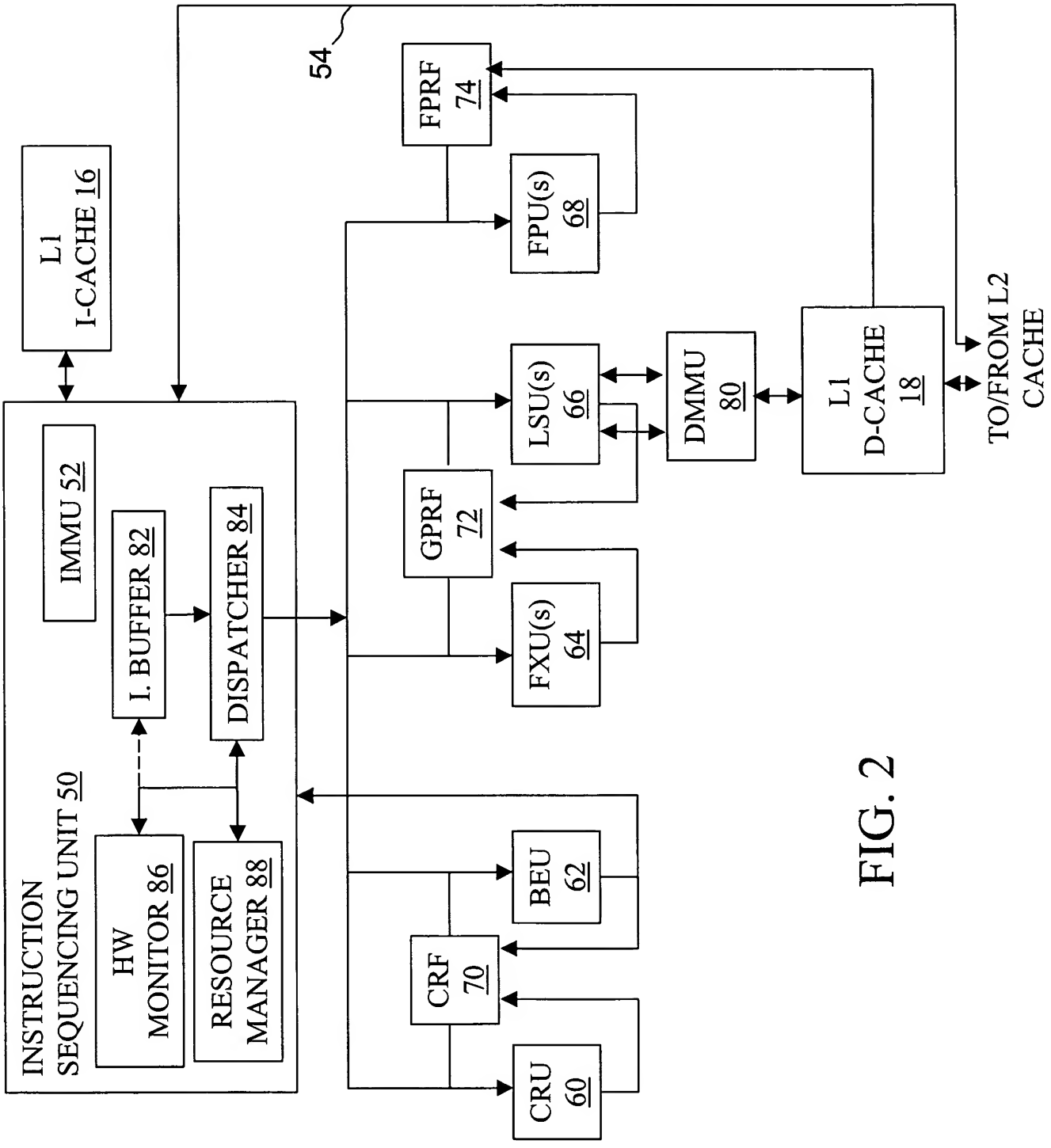

54
L1
I-CACHE 16
IMMU 52
I. BUFFER 82
DISPATCHER 84
INSTRUCTION
SEQUENCING UNIT 50
HW
MONITOR 86
RESOURCE
MANAGER 88
CRU
60
CRF
70
BEU
62
GPRF
72
FXU(s)
64
FPRF
74
FPU(s)
68
LSU(s)
66
DMMU
80
L1
D-CACHE
18
TO/FROM L2
CACHE

FIG. 2

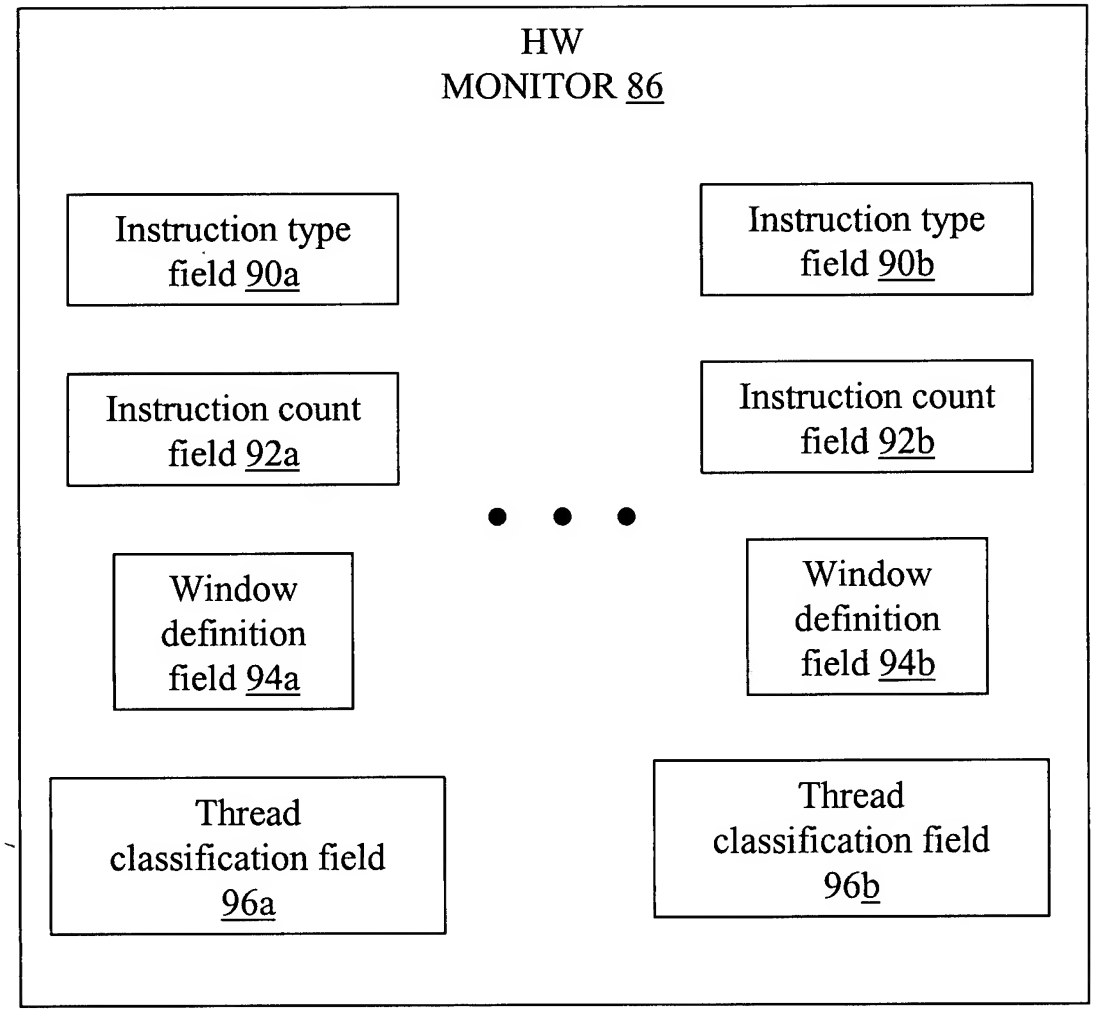

HW
MONITOR 86
Instruction type field 90a
Instruction type field 90b
Instruction count field 92a
Instruction count field 92b
Window definition field 94a
Window definition field 94b
Thread classification field 96a
Thread classification field 96b

FIG. 3A

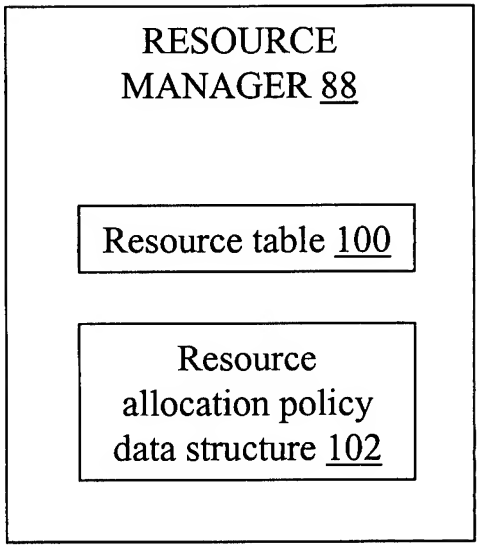

RESOURCE MANAGER 88
Resource table 100
Resource allocation policy data structure 102

FIG. 3B

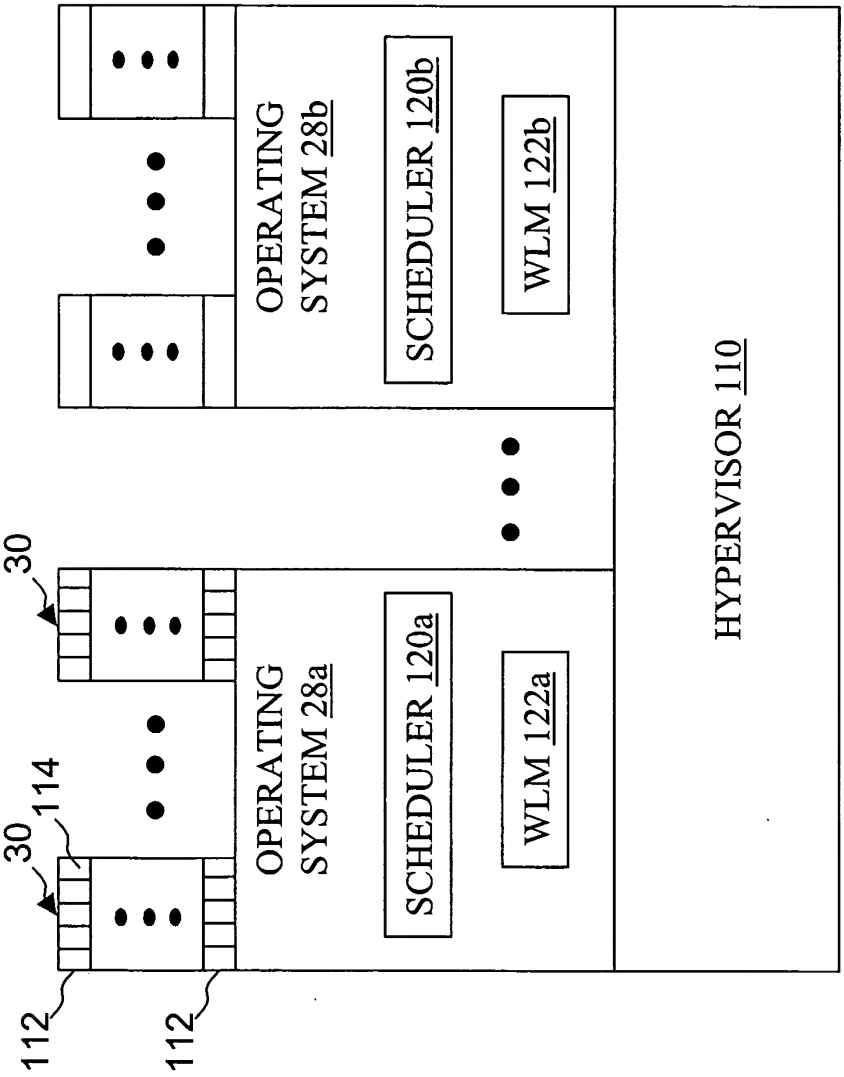
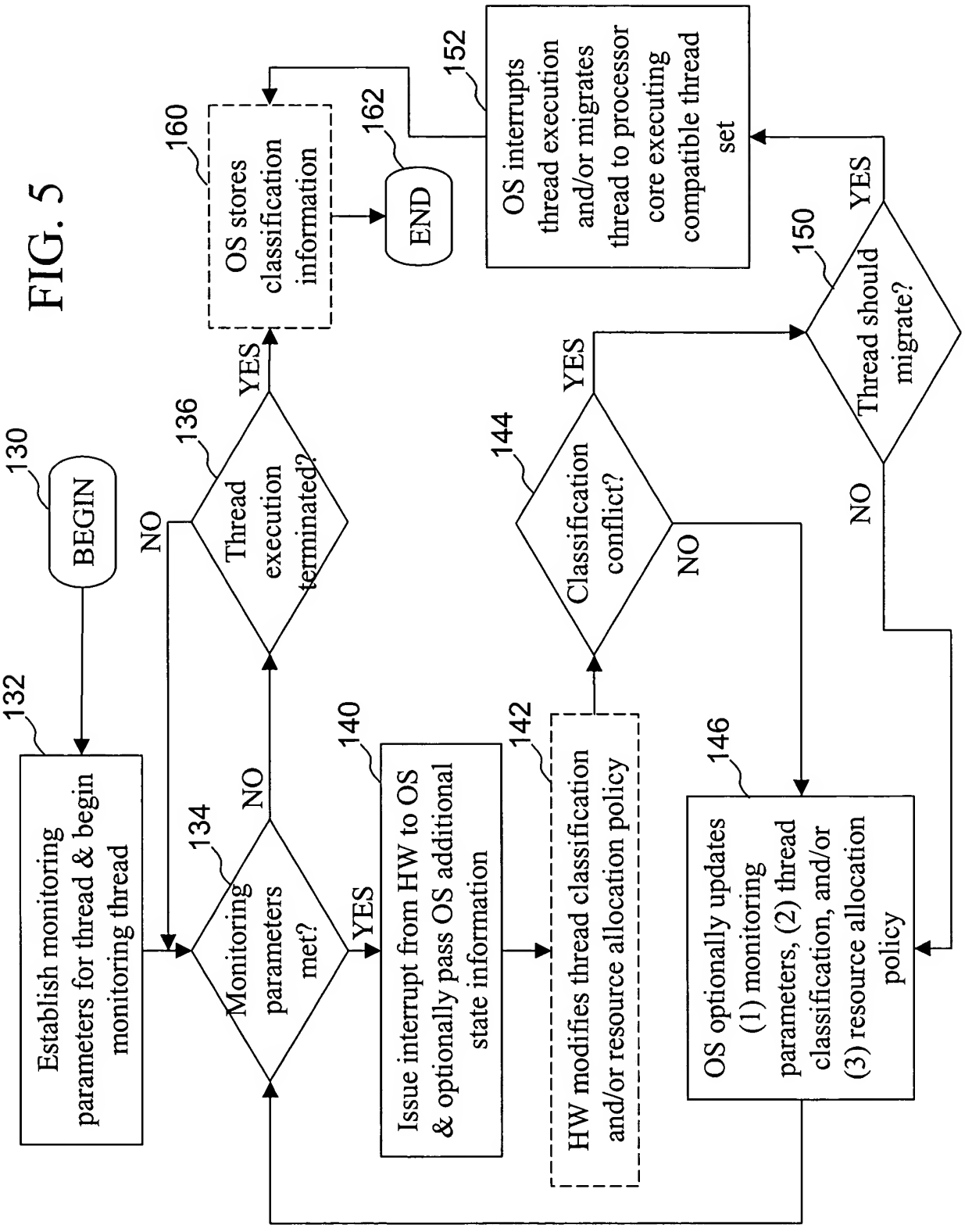

112
112
30
114
30
OPERATING SYSTEM 28a
SCHEDULER 120a
WLM 122a
OPERATING SYSTEM 28b
SCHEDULER 120b
WLM 122b
HYPERVISOR 110

FIG. 4

FIG. 5


130
BEGIN
132
Establish monitoring parameters for thread & begin monitoring thread
134
Monitoring parameters met?
NO
YES
136
Thread execution terminated?
NO
YES
140
Issue interrupt from HW to OS & optionally pass OS additional state information
142
HW modifies thread classification and/or resource allocation policy
144
Classification conflict?
YES
NO
146
OS optionally updates (1) monitoring parameters, (2) thread classification, and/or (3) resource allocation policy
150
Thread should migrate?
YES
NO
152
OS interrupts thread execution and/or migrates thread to processor core executing compatible thread set
160
OS stores classification information
162
END